



Digital to Analog – Digital to Analog (D/A) modules convert digital electrical signals to an analog signal. NAI offers for D/A smart function modules offering from four (high voltage) to sixteen output channels. The Dax smart function modules also include D/A FIFO buffering for greater control of the output voltage and signal data. Once enabled and triggered, the D/A FIFO buffer accepts, stores, and outputs the voltage (and/or current) commands for applications requiring simulation of waveform generation (single or periodic).

Module	Description
DA1	12 D/A Outputs (±10 VDC or ±25 mA)
DA2	16 D/A Outputs (+10 VDC or +10 mA)
DA3	4 (High Current) D/A Outputs (±40 VDC or +100 mA)
DA4	4 (High Voltage) D/A Outputs (+20 VDC to +80 VDC)
DA5	4 High-Voltage/High-Current (External VCC) D/A Outputs

Features

- High-quality D/A conversion, 16-Bit/channel
- Continuous background BIT
- External trigger/synchronization
- Automatic shutdown protection with the results displayed in a status word
- Extended D/A FIFO buffering capabilities

Built-In Test (BIT)/Diagnostic Capability

Two different tests, one online (D2) and one offline (D3), may be selected:

The online (D2) test initiates automatic background BIT testing, where each channel is checked to a test accuracy of 0.2% FS and monitored for shorted output. Any failure triggers an Interrupt (if enabled) with the results available in status registers. The testing is totally transparent to the user, requires no external programming, has no effect on the operation of this card and can be enabled or disabled via the bus.

The offline (D3) test uses an internal A/D that measures all D/A channels while they remain connected to the I/O and cycle through a number of signal levels. Each channel will be checked to a test accuracy of 0.2% FS. Test cycle is completed within 45 seconds and results can be read from the Status registers when D3 changes from 1 to 0. The test can be stopped at any time. This test requires no user programming and can be enabled or disabled via the bus.

New Embedded Soft Panel

North Atlantic Industries offers the newest cross platform (Windows and Linux) GUI for our Gen 5 products that allows a user to quickly interact with our broad range of modular, I/O cards and rugged embedded computing products. Embedded Soft Panel 2 (ESP 2) is coherent and easy to use with a clean, fleshed out UI with features such as drag and drop dock able windows, a dark and light theme, and multi-language support. Multiple ways to open a board are offered, including saving board opening settings for future use. Interacting with and collecting information on hardware is simple to do with the register editor for reading and writing specific addresses, and the API logger which logs all API library calls including their return status and parameters. ESP 2 has many new features and provides an organized and effortless interface for NAI's next generation products. Available for CentOS 7.4 and 8.2 and Windows 10 x64



D/A Example - Module DA1 Demo Mode Screen Shots

Basic DA		FIFO	O	Output Trigger		Watchdog		
Ch	Status En.	CBW Select	Mode	Polarity-Ran	ge (V/mA)	Set V/A	Wrap (V)	Wrap (mA)
1		3.3us 🔻	Voltage 🔽			0.0000		
2		3.3us 122us 1.32ms	Voltage 🔽			0.0000		
3		11.2ms 21ms	Voltage 🔽			0.0000		
4		3.3us 🔻	Voltage 🔽			0.0000		
5		3.3us 🔻	Voltage 🔽			0.0000		
6		3.3us 🔻	Voltage 🝷			0.0000		
7		3.3us 🔻	Voltage 🔽			0.0000		
8		3.3us 🔻	Voltage 🝷			0.0000		
9		3.3us 🔻	Voltage 🔽			0.0000		
10		3.3us 🔻	Voltage 🔽			0.0000		
11		3.3us 🔻	Voltage 🝷			0.0000		
12		3.3us 🔻	Voltage 🝷			0.0000		
All		3.3us 🔻	Voltage 🔽	Unipolar-1	.0 🔻	00.0000		

Basic DA		FIFO	FIFO Outpu		Watchdog					
Chan	Buffer Size	Buffer Ctrl	Delay	Freq	Software Trig		Count	AlmstEmpty	LowMark	HighMa
1	0.0000	Disabled 🔽	0.0000	0	DISABLE	•		0	0	
2	0.0000	1-Shot Repeat	0.0000	0	DISABLE	-		0	0	
3	0.0000	Disabled 🔻	0.0000	0	DISABLE	•		0	0	
4	0.0000	Disabled 🔻	0.0000	0	DISABLE	-		0	0	

Bas	sic DA		FIFO	Output Trigger
Ch	Set Output	Trig	Current Output	Trig.
	0 🔽			
	0 1 32			
	32 33 48			
	49			



Sm

Low Mark High D D D D D L D D D L D D D L D D D L D D D L D D D L D D D L D D D L D D D L D D D L D D D L D D D L D	FIFO	Status	
	OC	WDT	T
	4	4	4
	e	e	e
	7	7	7
	1	1	1
	12	12	12
r Clear Cle	A	A	A

Module Settings	Temperature Panel	Interrupts	FIFO Interrupts	BIT Tests		
Celsius 🖣	Current Core	Current Board	Max Core	Min Core	Max Board	Min Board
Motherboard						
Module						

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